

REMARKS

Status of the Application

Claims 23-45 are all the claims pending in the Application. Applicant thanks the Examiner for allowing claims 23-33.

Art Rejections

Claims 34-37, 44, and 45 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Rai et al.* U.S. Patent No. 4,818,728 ("*Rai*"). Claim 34 is an independent claim. Applicant respectfully traverses this rejection for at least the reasons stated below.

To be an "anticipation" rejection under 35 U.S.C. § 102, the reference must teach every element and recitation of the Applicants' claims. Rejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in the prior art. Thus, the reference must clearly and unequivocally disclose every element and recitation of the claimed invention.

Applicant submits that *Rai* fails to disclose at least the following recitations of independent claim 34:

bonding said second die to said first die such that the conductor on said first die is aligned with said conductor on said second die and said integral connection member on said first die connects to said second die in a coplanar state thus forming said dielectric package.

Rai is directed to a method of making a hybrid semiconductor device (*See e.g.; Title*). Specifically, Figures 1(a)-(c) depict a first and a second substrate 1/1 of the *Rai* invention. The corresponding description discloses that a plurality of electrodes 2/2 are deposited on the upper surfaces of the substrates 1/1 (*See Col. 3, lines 65-67*). Metal studs 4, having contact with the

deposited electrodes 2, are coupled to the first substrate 1 (*See Col. 4, lines 16-20*). To form the hybrid semiconductor device, the first 1 is placed above the second substrate '1 such that the metal studs 4 on the first semiconductor substrate 1 align with the respective solder deposits 5 on the second semiconductor substrate '1 (*See, Col. 4, lines 26-30*).

As clearly depicted in Figure 1(c), the first substrate 1 is thus connected to the second substrate '1 in a stacking or vertical manner. The description in *Rai* further discloses this architecture in describing that coupling the first semiconductor substrate 1 to the second semiconductor substrate '1 takes place by placing the first semiconductor substrate 1 on top of the second semiconductor substrate '1 (*See Col. 4, lines 25-30 and Col. 3, lines 3-7*). *Rai's* disclosure of coupling the two substrates together in a vertical fashion is completely different from the claimed subject matter which clearly recites that the first die connects to said second die in a coplanar state. In summary, because *Rai* does not disclose connecting the integral connection member on said first die to said second die in a coplanar state to forming said dielectric package as recited in independent claim 34, *Rai* cannot possibly anticipate the claimed subject matter. As such, the Examiner is respectfully requested to withdraw the § 102 rejection from independent claim 34 and from the claims that depend therefrom.

Claims 38-40, 42, and 43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Rai*, and further in view of *Tukamoto et al.* U.S. Patent No. 5,376,825 ("*Tukamoto*").

Claims 38-40, 42 and 43 respectively depend from independent claim 34. *Rai* is deficient with respect to independent claim 34 for at least the reasons stated above. Additionally, *Tukamoto* fails to fulfill the deficiencies of *Rai*.

Tukamoto is a standard interconnection technology, directed to a flexible integrated circuit package for computer systems, which would not be of any use at the high frequencies that

the dielectric package of the instant Application is designed to be useful with. *Tukamoto* does not disclose, teach or suggest connecting the integral connection member on said first die to said second die in a coplanar state thus forming said dielectric package.

Without at least such a suggestion, one would not have been motivated to combine the method of making a hybrid semiconductor device, as disclosed in *Rai*, with the integrated circuit package, as taught in *Tukamoto*, to produce the claimed subject matter. Because there can be found in *Tukamoto* no teaching or suggestion that meets the above-identified limitations, the combination of *Rai* and *Tukamoto* cannot reasonably be said to render obvious the claimed subject matter. The Examiner is therefore respectfully requested to withdraw the § 103(a) rejection from independent claim 34 and from the claims that depend therefrom.

Claim 41 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Rai*, in view of *Tukamoto*, and further in view of *Kazior et al., DBIT - Direct Backside Interconnect Technology: A Manufacturable, Bond Wire Free Interconnect Technology for Microwave and Millimeter Wave MMICs* ("*Kazior*").

Claim 41 ultimately depends from independent claim 34. *Rai* is deficient with respect to independent claim 34 for at least the reasons stated above. Additionally, *Kazior* fails to fulfill the deficiencies of *Rai*.

Kazior is directed to the manufacturing of a bond wire free chip interconnect technology. However, *Kazior* does not disclose, teach or suggest connecting the integral connection member on said first die to said second die in a coplanar state thus forming said dielectric package.

Without at least such a suggestion, one would not have been motivated to combine the method of making a hybrid semiconductor device, as disclosed in *Rai*, with the direct backside interconnect technology, as taught in *Kazior*, to produce the claimed subject matter. Because

there can be found in *Kazoir* no teaching or suggestion that meets the above-identified limitations, the combination of *Rai* and *Kazior* cannot reasonably be said to render obvious the claimed subject matter. The Examiner is therefore respectfully requested to withdraw the § 103(a) rejection from independent claim 34 and from the claims that depend therefrom.

Conclusion

In view of the foregoing, it is respectfully submitted that claims 23-45 are allowable. Thus, it is respectfully submitted that the application now is in condition for allowance with all of the claims 23-45.

If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Please charge any fees which may be required to maintain the pendency of this application, except for the Issue Fee, to our Deposit Account No. 19-4880.

Respectfully submitted,



Timothy P. Cremen
Registration No. 50,855

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

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Date: January 20, 2004